LISTING OF CLAIMS

1. (Currently Amended) A method for depositing a diffusion barrier and a metal conductive layer for metal interconnects on a substrate, the method comprising:

(a) etching the bottoms of recessed features on a surface of the substrate to clean at least part of an underlying metal while simultaneously depositing a first portion of a diffusion barrier on at least sidewalls of recessed features, wherein depositing a first portion of a diffusion barrier comprises sputtering metal from a target;

(b) depositing a second portion of the diffusion barrier, which covers at least the bottoms of the recessed features; and

(c) depositing the metal conductive layer over the surface of the substrate.

2. (Original) The method of claim 1, wherein the method does not employ a precleaning operation prior to (a).

3. (Original) The method of claim 1, further comprising, after (b) and prior to (c), etching the second portion of the diffusion barrier at least at the bottoms of the recessed features without exposing an underlying metal.

4. (Original) The method of claim 1, further comprising performing a degas operation prior to (a).

5. (Original) The method of claim 1, wherein at least some of the recessed features have aspect ratios of not greater than about 2.

6. (Original) The method of claim 1, wherein the recessed features are trenches of a single Damascene structure.

7. (Original) The method of claim 1, wherein at least operations (a) and (b) are performed in the same processing chamber.

8. (Original) The method of claim 7, wherein the processing chamber is a plasma physical vapor deposition (PVD) chamber.

9. (Original) The method of claim 7, wherein the processing chamber comprises a hollow cathode magnetron.

10. (Original) The method of claim 4, wherein the substrate is degassed by heating the substrate to between about 150 to 400 degrees Celsius.

11. (Original) The method of claim 1, wherein (a) comprised etching the bottoms of recessed features to a depth of about 20 to 100 Angstroms into the underlying metal.

12. (Original) The method of claim 1, wherein (a) comprises etching under conditions producing an etch-to-deposition ratio ranging between about 1 and 1.5 in field regions of the substrate and an etch-to-deposition ratio ranging between about 1.1 and 3 in the bottoms of the recessed features.

13. (Original) The method of claim 1, wherein (a) comprises depositing the first portion of diffusion barrier elsewhere on the substrate to a thickness of between about 10 and 100 Angstroms on field regions of the substrate and sidewalls of the recessed features.

14. (Original) The method of claim 1, wherein (b) comprises depositing the second portion of diffusion barrier to a thickness of at least about 5 Angstroms on the bottoms of the recessed features.

15. (Original) The method of claim 1, wherein (a) comprises sputtering a metal from a target having an applied DC power of between about 1 and 10 kW and biasing the substrate with about 200 to 2000 W of RF power.

16. (Original) The method of claim 1, wherein (b) comprises using chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), or pulsed deposition layer (PDL).

17. (Original) The method of claim 1, wherein at least one portion of the diffusion barrier comprises a material selected from the group consisting of tantalum, nitrogen-doped tantalum, tantalum nitride, titanium nitride, tungsten nitride, ruthenium, and silicon containing versions of any of these.

18. (Original) The method of claim 1, wherein (a) comprises sputtering a metal from a target having an applied DC power of between about 1 and 30 kW, while applying a bias to the substrate.

19. (Original) The method of claim 18, wherein the bias comprises RF power of between about 100 and 2000 W.

20. (Original) The method of claim 18, wherein (a) further comprises passing argon gas through the process chamber at a flow rate of between about 10 and 300 sccm.

21. (Original) The method of claim 1, wherein the metal conductive layer of (c) comprises copper.

22. (Original) The method of claim 21, wherein the metal conductive layer is a copper seed layer.

23. (Original) A method of claim 1, further comprising, prior to (a), depositing a portion of the diffusion barrier on the surface of the partially fabricated integrated circuit such that the sidewalls of the recessed features have a diffusion barrier thickness of between about 5 and 100 Angstroms.